Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Claim 4 has been amended.

Listing of Claims:

1. (Previously Amended): A method, comprising:

determining a bootstrap processor from a plurality of operable processors in a fault tolerant multiprocessor system irrespective of an initialization time of a particular operable processor;

asserting a first signal;

asserting a second signal; and

ensuring that both the first signal and the second signal are asserted prior to allowing the plurality of operable processors to enter a bootstrap processor arbitration process.

2. (Canceled)

3. (Previously Amended): The method of claim 1, wherein the first signal indicates that a particular processor has successfully completed an initialization sequence, and the second signal indicates that all of the operable processors in the fault tolerant multiprocessor system are ready to enter the bootstrap processor arbitration process.

4. (Currently Amended): The method of claim 1, wherein the second signal is communicated across [the] a system bus to each processor.

5. (Previously Amended): The method of claim 1, wherein asserting is selected from one in a group consisting of driving a signal line to a logical 0, driving the signal line to a logical 1, toggling the signal line from a logical 1 to a logical 0, and driving the system bus to a logic state on a first clock cycle and releasing the system bus on a second clock cycle.

6. (Previously Amended): The method of claim 1, wherein the fault tolerant multiprocessor system comprises a multiprocessor system which continues to be operable irrespective of a fault occurring in any particular processor.

7. (Previously Amended): The method of claim 1, wherein the operable processor comprises a processor which has successfully completed an initialization and testing sequence.

8-12. (Canceled)

13. (Previously Amended): A computing system, comprising:

a plurality of operable processors;

a system bus;

an arbitration protocol to determine a bootstrap processor from the plurality of operable processors in a fault tolerant multiprocessor system irrespective of an initialization time of a particular operable processor; and

logic to ensure that both a first signal and a second signal are asserted prior to allowing the plurality of operable processors to enter a bootstrap processor arbitration process.

14. (Original): The computing system of claim 13, wherein the arbitration protocol comprises micro code instructions.

15. (Original): The computing system of claim 13, wherein the arbitration protocol comprises logic circuitry located in a processor.

16. (Original): The computing system of claim 13, wherein the arbitration protocol conducts the bootstrap processor arbitration process across the system bus.

17. (Original): The computing system of claim 13, wherein each of the operable processors has a bus controller, the bus controller to stall transactional activity on the system bus until the bootstrap processor determination has been made.

18. (Previously Amended): An apparatus, comprising:

a computer readable media; and

instructions embedded on the computer readable media, the instructions when executed by a machine, cause the machine to perform operations comprising:

determining a bootstrap processor from a plurality of operable processors in a fault tolerant multiprocessor system irrespective of an initialization time of a particular operable processor;

asserting a first signal;

asserting a second signal; and

ensuring that both the first signal and the second signal are asserted prior to allowing the plurality of operable processors to enter a bootstrap processor arbitration process.

19. (Canceled)

20. (Previously Amended): The apparatus of claim 18, wherein the first signal indicates that a particular processor has successfully completed an initialization sequence, and the second

signal indicates that all of the operable processors in the fault tolerant multiprocessor system are ready to enter the bootstrap processor arbitration process.

21. (Previously Amended): The apparatus of claim 18, wherein the first signal indicates that a particular processor has been assigned an arbitration identification number.

22. (Previously Amended): The apparatus of claim 18 wherein the instructions comprise micro code.